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Seat No.	

T.E. (Electronics) (Semester - V)
Examination, April - 2018
SIGNALS AND SYSTEMS
Sub. Code :66280

Day and Date : Tuesday, 24- 4 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 1.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Figures to the right indicates full marks.**
3) **Assume necessary data wherever required.**

SECTION - I

Q1) Solve any two. **[16]**

a) Draw even and odd parts of following signals.

i) $x(t) = 1$ for $-1 \leq t \leq 1$

$= -1$ for $1 \leq t \leq 2$

$= 0$ otherwise

ii) $x[n] = [1.5, 2, 1, 2, 1.5]$ (↑ at the first sample)

b) Find the convolution integral of the following signals and plot resultant sketch.

$x(t) = u(t) - u(t-4)$ and $h(t) = u(t) - u(t-1)$

c) Determine whether the following LTI systems are causal or not.

i) $h(t) = e^{-3t}.\ u(t-1)$

ii) $h[n] = (0.5)^n.\ u[n+3]$

Q2) Solve any two. **[16]**

a) Determine whether the following signals are energy signal, power signal or neither of two.

i) $x(t) = \sin(2t)$

ii) $x[n] = \cos(\pi n)$ for $-4 \leq n \leq 4$ and zero otherwise

P.T.O.

b) Find the convolution sum of the following signals and find values for $n = -5$, $n = 5$ and $n = 10$ $x[n] = u[n]$ and $h[n] = \left(\frac{3}{4}\right)^n u[n]$

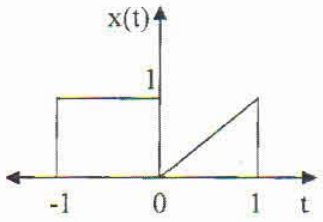
c) A signal x(t) is as shown in fig. Sketch and label each of the following.

i) $x(1 - t)$

ii) $x(t - 1)$

iii) $x(2t + 2)$

iv) $x(2 + t/2)$



Q3) Solve any three. **[18]**

a) State and explain sampling theorem.

b) With a neat schematic explain aliasing effect.

c) Determine whether the following signals are periodic or nonperiodic. If periodic find fundamental period.

i) $x[n] = 5\cos\left[\frac{\pi n}{2}\right] - \sin\left[\frac{\pi n}{8}\right] + 3\cos\left[\frac{\pi n}{4} + \frac{\pi}{4}\right]$

ii) $x(t) = 2\cos(t) + \sin\left(\sqrt{2}t\right)$

d) Define and explain all properties of systems.

SECTION - II

Q4) Attempt any two. **[18]**

a) What are the properties of DFT? Prove any one.

b) Find 4 point DFT of the following sequence $x(n) = \{\underset{\uparrow}{1}, -2, 3, 4\}$.

c) Find the Fourier Transform of the following.

i) $a^n\, u(n)$

ii) $\delta(n+2) - \delta(n-2)$

Q5) Attempt any two. **[16]**

a) Find the 2 transform of the following

i) $x(n) = u(n) - 4\ (n-3)$

ii) $x(n) = \{1, 2, 3, 2\}$

b) What is ROC? Explain the properties of ROC.

c) Find the inverse z transform of $x(z) = \frac{¼z^{-1}}{(1-½z^{-1})(1-¼z^{-1})}$; Roc: $|z| > ½$.

Q6) Attempt any two. **[16]**

a) Obtain the direct form - I realization for the system described by the difference equation. $y(n) - \frac{5}{6}y(n-1) + \frac{1}{6}y(n-2) = x(n) + 2x(n-1)$.

b) Obtain the direct form II realization of the LTI system governed by the equation,

$$y(n) = -\frac{3}{8}y(n-1) + \frac{3}{32}y(n-2) + \frac{1}{64}y(n-3) + x(n) + 3x(n-1) + 2n(n-2).$$

c) Find the z transform of $n(n) = \left(\frac{2}{3}\right)^n u(n) + \left(-\frac{1}{2}\right)^n u(n)$. Determine the ROC and pole zero locations.

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T.E. (Electronics Engineering) (Part - III) (Semester - V) (Revised) Examination, April - 2018

MICROCONTROLLER

Sub. Code : 66281

Day and Date : Wednesday, 25 - 4 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 1.00 p.m.

Instructions : 1) **All questions are compulsory.**
2) **Assume suitable data if necessary.**
3) **Figures to right indicate full marks.**

SECTION - I

Q1) Answer any three of the following. **[18]**

a) Explain TCON register of MCS 8051.

b) Explain read modify write feature & list all read modify write instructions.

c) Explain all Conditional branch Instructions of 8051.

d) Explain single stepping operation with respect to interrupt of MCS 8051.

Q2) Answer any two of the following. **[16]**

a) Explain various timer modes of 8051.

b) Explain program memory organization & data memory organization of MCS 51.

c) Explain IP Register & IE Register of 8051.

Q3) Answer any two of the following. **[16]**

a) Explain various Serial communication modes and comment on baud rate in each mode.

b) Interface four digit 7 Segment displays (Common Anode Type) with MCS 8051 and write assembly language program to display message "8051".

c) Explain PCON register in detail.

P.T.O.

SECTION - II

Q4) Answer any three of the following. **[18]**

a) Explain various C data types.

b) Write a 8051 C Program to get a data byte from port P1, wait half Second and then send it to port P2.

c) Explain configuration word of PIC 16f877.

d) What is oscillator start up timer and power up timer, explain their significance.

Q5) Answer any two of the following. **[16]**

a) Explain timer 1 and T1CON register of PIC 16f877.

b) Write assembly language program to blink LED connected to PC0 Pin of PIC 16f877.

c) Explain PSP mode of PIC 16f877 and also comment on IBF, OBF and IBOE status bits of TRISE register.

Q6) Answer any two of the following. **[16]**

a) Explain PWM module of PIC 16f877.

b) Explain Interrupt structure of PIC 16f877.

c) Explain Sleep mode of PIC 16f877.

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Seat No.	

T.E. (Electronics) (Semester - V) (New) Examination, April - 2018
ELECTROMAGNETIC ENGINEERING
Sub. Code : 66282

Day and Date : Thursday, 26 - 4 - 2018 **Total Marks : 100**
Time : 10.00 a.m. to 1.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Figures to the right indicates full marks,**
3) **Assume suitable data if necessary.**
4) **Use non-programmable calculator.**

SECTION-I

Q1) Attempt any two: **[16]**

a) Explain the following terms:
   i) Flux density.
   ii) Coulomb's law and electric field.

b) State and prove Divergence theorem.

c) Point charges of 50 nc each are located at A(1, 0, 0), B(–1, 0, 0), C(0, 1, 0) and D(0, –1, 0) in free space. Find the total force on the charge at A.

Q2) Attempt any two: **[16]**

a) Give Maxwell's equations for time varying fields.

b) Derive the expression for Electrostatic potential.

c) A dipole moment $\bar{p} = 6\overline{a_z}$ nc–m is located at the origin in free space
   i) Find V at P(r = 4, θ =20°, ϕ = 0°)
   ii) Find $\bar{E}$ at p.

Q3) Attempt any Three: **[18]**

a) Torque on loop.

b) Stoke's Theorem.

c) Potential Gradient.

d) Find total charge enclosed if

$$D = e^{-x} \sin y\, \overline{a_x} - e^{-x} \cos y\, \overline{a_y} + 2z\overline{a_z} \text{ c/m}^2$$

P.T.O.

SECTION-II

Q4) Attempt any two: **[16]**

a) Derive the expression for attenuation constant α and phase shift constant β for conducting media.

b) Explain power flow in uniform plane wave and give circuit applications of the poynting vector.

c) The parameters of a certain transmission line operating at 6×10^8 rad/s are L = 0.4 μH/m, C = 40 pf/m, G = 80 μs/m and R = 20 Ω/m. Find γ and Z_0.

Q5) Attempt any two: **[16]**

a) Explain in detail transmission line parameters.

b) What is stub matching? Why it is needed? Explain.

c) The electric field amplitude of a uniform plane wave propagating in the $\overline{a_z}$ direction is 250 v/m. If $\overline{E} = E_x \overline{a_x}$ and w = 1.00 Mrad/s, find

i) the frequency

ii) the wavelength

iii) the period

iv) the amplitude of $\overline{H}$

Q6) Attempt any Three: **[18]**

a) Characteristics impedance Z_0.

b) Polarization.

c) Smith chart.

d) The characteristic impedance of a certain lossless transmission line is 72 Ω. If L = 0.5 μH/m, find capacitance C.

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Total No. of Pages : 2

T.E. (Electronics) (Semester - V) (Revised) Examination, April - 2018
VLSI DESIGN
Sub. Code :66283

Day and Date : Friday, 27- 4 - 2018 **Total Marks : 100**
Time : 10.00 a.m. to 1.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Figures to the right indicates full marks.**
3) **Assume suitable data if required.**

SECTION - I

Q1) Attempt any three. **[3×6=18]**

a) Write a VHDL description to implement with D-FF with synchronous reset.

b) Write a VHDL description to implement 4-bit 2-input multiplexer.

c) Explain the syntax for physical literals. Describe Current (nA, μA, mA, A) as physical type.

d) What is meta stability and synchronizer failure? Explain in brief with neat diagrams.

Q2) Attempt any two. **[2×8=16]**

a) What is concurrent statement? List and explain the syntax of 'when-else' and 'with select' statement.

b) Write VHDL description for 8: 1 Mux using 'with select' statement

c) Write a VHDL structural description to implement 4:1 mux using 2:1 mux.

P.T.O.

Q3) Attempt any two. **[2×8=16]**

a) Design a Moore machine to detect non overlapping sequence '101' sequence and describe it using VHDL.

b) Design a 4 bit shift register with shift enable and shift left or shift right controls and describe it using VHDL.

c) Design a FSM to produce a sequence 1.3,7,9,11,13,15,17 describe it using VHDL.

SECTION - II

Q4) Attempy any three. **[3×6=18]**

a) Explain 'block' and 'arrayl' attributes with example.

b) Explain with example WAIT statements in VHDL.

c) Explain with example fault models for testing.

d) What is JTAG? Explain the JTAG standard and interface.

Q5) Attempt any two. **[2×8=16]**

a) Explain with neat diagram structure of IOB spartan - II FPGA.

b) Write a algorithm and design the datapath for n Factorial and list control words.

c) Design a control unit for simple IF – THEN–ELSE algorithm.

Q6) Attempt any Two. **[2×8=16]**

a) List various features of spartan - II LUT and details of BLOCK RAM.

b) With neat diagram explain boundary scan testing technique.

c) Draw and explain architecture, features of XC95xx series CPLD.

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Seat No.	

T.E. (Electronics) (Part - III) (Semester - V) (Revised) Examination, April - 2018

DIGITAL COMMUNICATION

Sub. Code : 66284

Day and Date : Saturday, 28 - 04 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 1.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data if necessary.**

Q1) Solve any two of the following: **[18]**

a) In an experiment of drawing a card from a well shuffled pack, all the elementary events are equally likely. If the event of getting a Heart is denoted by H, and that of an ace is denoted by A,explain the events $H \cap A$, $H \cup A$ and find their probabilities.

b) A pair of fair dice is rolled, the values of their faces are added; and sum of faces and probabilities are noted down. Draw the distribution function associated with the experiment.

c) Define joint probability density function & mention the properties of joint probability density function of two random variables.

Q2) Solve any two: **[16]**

a) Explain in detail non uniform quantization.

b) In a pcm, using n-bits encoder. Show that signal to quantization noise ratio is given as (1.8 +6N) dB for sine wave input.

c) Draw the block diagram of Adaptive delta modulation and explain in detail.

P.T.O.

Q3) Solve any two: **[16]**

a) Draw the waveforms of Adaptive delta modulation & Linear delta modulation & compare their response & comment on it.

b) Represent the data 101101001 using following data formats with the help of waveforms.

i) Bipolar RZ.

ii) Bipolar NRZ.

iii) Unipolar RZ.

iv) Split phase manchester format.

c) Explain carrier recovery circuit.

Q4) Solve any two: **[16]**

a) Explain the QPSk modulation scheme with suitable transmitter and receiver block diagram.

b) With the help of neat block schematic & space diagram explain the QAM transmitter & receiver.

c) Explain Coherent Binary Phase shift keying.

Q5) Solve any two: **[16]**

a) What do you understand by inter symbol interference? What are its effects? How can ISI be reduced. (Intersymbol Interference).

b) Discuss the properties and applications of matched filter.

c) Explain with circuit diagram Early-Late bit symbol synchronization.

Q6) Solve any two: **[18]**

a) List out and prove the properties of Pseudo-random sequences used in CDMA systems.

b) Explain the concept of spread spectrum modulation and list characteristics of SS signal.

c) Explain how integration is used to detect baseband signal. Obtain an expression for signal to noise ratio integrate and dump receiver.

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Seat No.	

T.E. (Electronics) (Part - III) (Semester - V) Examination, April - 2018

CONTROL SYSTEM ENGINEERING

Sub. Code : 45593

Day and Date : Saturday, 28 - 04 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data, if necessary.**
4) **Use of graphs are allowed.**

SECTION - I

Q1) Solve any two (9 marks each) **[18]**

a) A unity feedback system has $G(S) = \dfrac{16}{S(S+5)}$

If a step I/P is given calculate

i) Damping ratio ii) Overshoot

iii) Settling time

b) State & derive the steady state errors & error constants for Type 0, Type 1 & Type 2 system.

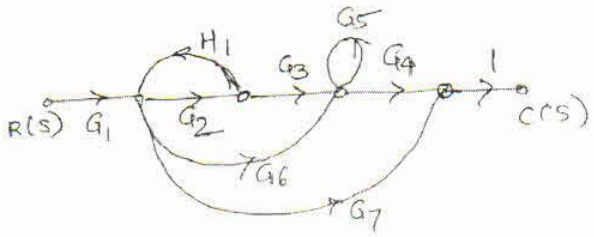
c) Explain block diagram reduction rules.

Q2) Solve any two (8 marks each) **[16]**

a) Describe the time response of 1st order system to unit step signal.

b) Describe transfer function of field controlled D.C. motor.

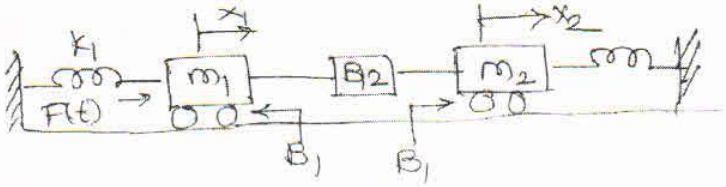
c) Obtain the overall transfer function C/R from the signal Flow graph shown in Fig. below.



P.T.O.

Q3) Solve any two (8 marks each) [16]

a) Draw the F-I & F-V analogous Ckts.



b) Compare open loop & closed loop systems along with examples.

c) Explain Routh-Hurwitz stability criterion.

SECTION - II

Q4) Solve any two (9 marks each) [18]

a) Draw Bode plot for the system $G(S) = \dfrac{80}{S(S+2)(S+20)}$

Determine G.M., P.M., W_{gc} & W_{pc}. Comment on stability.

b) Sketch the root locus of feedback system whose open loop transfer function is given by $G(S)H(S) = \dfrac{k}{S(S+2)(S+3)}$

c) Explain root locus technique. Discuss the root locus construction rules.

Q5) Solve any two (8 marks each) [16]

a) Explain lead-lag compensator. Discuss the steps to design a lead-lag compensator.

b) A system is described by

$$X = \begin{bmatrix} 1 & -1 \\ 1 & -1 \end{bmatrix} X + \begin{bmatrix} 0 \\ 1 \end{bmatrix} u$$

$Y = [1\ 0]x$

check controllability & observability of the system.

c) Explain PID controller with suitable block diagram.

Q6) Solve any two (8 marks each) [16]

a) Explain with neat diagram the concept of ladder diagram for PLC.

b) Derive state model in canonical form. For a given general transfer function & show it in block diagram form.

c) Describe Nyquist stability criterion

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Seat No.	

T.E. (Electronics Engineering) (Part-III) (Semester - VI) (Revised) Examination, May - 2018

VIDEO ENGINEERING

Sub. Code : 66852

Day and Date : Saturday, 05 - 05 - 2018 **Total Marks : 100**

Time : 2.30 p.m. to 5.30 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Use suitable assumptions if required.**
3) **Draw necessary figures on right side of answer sheet.**

SECTION-I

Q1) Solve any three: **[18]**

a) Explain positive and negative modulation with suitable waveforms.

b) Draw the block diagram of PAL decoder and write function of each blocks.

c) Explain aspect ratio, horizontal and vertical resolution, and video bandwidth for TV.

d) Explain the factors on which Channel Bandwidth for video broadcasting depends.

e) Draw suitable diagram and explain microphone and speaker.

Q2) Solve any two: **[16]**

a) What is equalizer & mixer. Explain with suitable application.

b) What is Scanning? State and explain advantages of Interlace scanning.

c) Draw and explain Composite video signal for chess board pattern.

Q3) Solve any two: **[16]**

a) Explain optical recording and reproduction.

b) Compare NTSC and SECAM T.V. system.

c) Draw suitable diagram and explain different elements of Colour picture tube.

P.T.O.

SECTION-II

Q4) Answer any three sub Questions: **[18]**

a) Describe briefly the merits of digital TV receivers that are not achievable in analog receivers.

b) Draw the structure of the plasma display panel (PDP) used for Television and explains it's working.

c) Explain the Multiple sub-Nyquist sampling encoding developed for HDTV.

d) Draw the basic block diagram of an up-link setup and explain how the signals are Compressed, packetized and multiplexed before modulation and transmission.

Q5) Answer any two sub Questions: **[16]**

a) Draw the block diagram of video codec VCU 2134 and explain digital signal processing carried out in it (I T T).

b) Draw and explain the working of different types of LCD Matrix used for television.

c) Describe the merits and applications of CATV system. Draw a typical layout of this system of signal distribution. Why are the amplifiers and equalizers required along trunk distribution lines?

Q6) Answer any two sub Questions: **[16]**

a) Draw and explain D_2 MAC baseband signal waveform for normal unscrambled picture transmission.

b) Draw and explain the construction of LCD panels used for the television.

c) What are the features and functions of CCTV with suitable diagram? Explain any one application of the CCTV?

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Seat No.	

T.E. (Electronics) (Semester - VI) (Revised) (New) Examination, May - 2018

DIGITAL SIGNAL PROCESSING

Sub. Code : 66851

Day and Date : Thursday, 03 - 05 - 2018 **Total Marks : 100**

Time : 2.30 p.m. to 5.30 p.m.

Instructions : 1) **Figures to right indicate full marks.**
2) **Assume suitable data if required.**

SECTION - I

Q1) Attempt any two: [18]

a) Explain in detail Radix 2, DIF FFT Algorithm.

b) Explain in detail Overlap add method of sectioned Convolution.

c) State and prove any four properties of DFT.

Q2) Attempt any two: [16]

a) Compare DFT, Z Transform and Wavelet Transform.

b) Write a note on 'Applications of Wavelet Transform'.

c) What are the properties of Wavelet Transform? Explain.

Q3) Attempt any two: [16]

a) Explain the procedure for designing FIR filter by Fourier Series Method.

b) Explain in detail necessary and sufficient condition for the linear phase characteristic of an FIR Filter? What are the advantages and disadvantages of FIR Filter?

c) Explain in detail design of FIR filter using windows.

P.T.O.

SECTION - II

Q4) Attempt any two: **[18]**

a) Explain in detail Bilinear Transformation Method.

b) Write the procedure for the design of low pass digital Butterworth IIR Filter.

c) Convert the analog filter with the system function H(s) given below into digital filter using bilinear transformation. Take T = 0.5. $H(s)\frac{s+0.3}{(s+0.3)^2+16}$.

Q5) Attempt any two: **[16]**

a) Write a note on 'Architecture of TMS320C67XX'.

b) Explain in detail finite word length effect in Digital filters.

c) Explain in detail FIR and IIR Filter Realization Schemes.

Q6) Attempt any two: **[16]**

a) Write a note on 'Sampling rate conversion by I/D factor'.

b) Explain in detail Two Stage Interpolator.

c) Explain the need of Multi-rate DSP. What is up sampling and Down Sampling? Explain.

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Seat No.	

T.E. (Electronics) (Semester - V) (Pre-Revised) (Old) Examination, May - 2018
DIGITAL SYSTEM DESIGN
Sub. Code: 45591

Day and Date : Saturday, 19 - 05 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 1.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data if required.**

SECTION - I

Q1) Attempt any three: **[3 × 6 = 18]**

a) Compare signal & variable in VHDL.

b) What is the significance of architecture in VHDL, also explain its types.

c) What is the significance of "*port map*" in VHDL? Give example.

d) Write a VHDL code for 8:1 multiplexer, using *case* statement.

Q2) Attempt any two: **[2 × 8 = 16]**

a) Write a VHDL code for full adder using half adder as component.

b) Write a VHDL code for SISO shift register to shift the data towards left by 1-bit.

c) Write a VHDL code for binary up-down counter.

Q3) Attempt any two: **[2 × 8 = 16]**

a) Draw and explain VLSI design flow.

b) Design sequence detector for detecting the sequence 011.

c) How to interface the asynchronous inputs with synchronous system.

P.T.O.

SECTION - II

Q4) Attempt any three: **[3 × 6 = 18]**

a) Write a note signal and array attributes.

b) What are the drawbacks of stuck at fault model? Explain in detail the path sensitizing model.

c) Draw the explain function block of XC95XX CPLD.

d) Explain event driven simulator.

Q5) Attempt any two: **[2 × 8 = 16]**

a) Draw and explain the IOB of Spartan-II FPGA.

b) Draw and explain *built in self test* testing technique.

c) Design the datapath for processor having instructions like IN, OUT, DEC, JNZ & HALT.

Q6) Attempt any two: **[2 × 8 = 16]**

a) Explain control unit designing for EC-1 GPP.

b) Draw and explain architecture of IOB of XC9572 CPLD.

c) What do you mean by delay? Explain inertial & transport delay.

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Seat No.	

T.E. (Electronics) (Part-III) (Semester - VI) (New) (Revised) Examination, May - 2018

POWER ELECTRONICS

Sub. Code : 66853

Day and Date : Tuesday, 08 - 05 - 2018 **Total Marks : 100**

Time : 2.30 p.m. to 5.30 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Draw neat circuit diagrams and waveforms wherever necessary.**
3) **Figures to the right indicate full marks.**

Q1) Attempt any two of the following: **[16]**

a) State different turn-on methods of SCR and explain gate turn on method with neat circuit diagram.

b) Draw and explain construction and characteristics of IGBT.

c) Draw and explain gate trigger characteristics of SCR.

Q2) Attempt any two of the following: **[16]**

a) What is the need of synchronization of control and power circuit in controlled rectifiers. Draw and explain line synchronized UJT triggering circuit?

b) Explain the different types of isolation circuits. What is the need of such circuits when motors are driven by power electronic circuits.

c) Draw and explain microprocessor based firing scheme for single phase full converter.

Q3) Attempt any two of the following: **[18]**

a) Draw and explain the operation of single phase full bridge converter with RL load for contineous and discontineous currents.

b) Draw the Diac-triac phase controlled circuit and explain its operation with waveforms.

P.T.O.

c) A single phase semiconverter operated from 230 V at 50 Hz, if $\alpha = 45°$. Find out:

i) Average output voltage
ii) RMS output voltage
iii) Form factor
iv) Ripple factor

Q4) Attempt any two of the following: **[16]**

a) How the choppers are classified. Explain the classification in details.

b) Draw the circuit diagram of a step up chopper and derive its equation for o/p voltage.

c) A DC chopper of input voltage 200 V remains on for 25 m.sec and off for 10 m.sec. Determine the average voltage which appears across the load. If the load is assumed to be resistive (R = 10 ohms), then find the RMS value of output voltage and power delivered to the load.

Q5) Attempt any two of the following: **[16]**

a) What is the principle of operation of an inverter? Explain in detail operation of single phase full bridge inverter with R-load & also derive the equation of rms output voltage?

b) What are the techniques for harmonic reduction. Explain any one technique in details.

c) What are the types of Inverter. Explain the different performance parameters of Inverter.

Q6) Attempt any three of the following: **[18]**

a) Draw the diagram of constant voltage transformer & explain its operation.

b) With neat block diagram explain online and offline UPS.

c) Derive the expression for heat developed in a material by induction heating. What factors decide the depth of penetration?

d) Explain in detail battery charger circuit.

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Seat No.	

T.E. (Electronics) (Semester - VI)
Examination, May - 2018
COMPUTER ARCHITECTURE AND OPERATING SYSTEM
Sub. Code : 66854

Day and Date : Saturday, 12 - 05 - 2018 **Total Marks : 100**

Time : 2.30 p.m. to 5.30 p.m.

Instructions : 1) **All questions are compulsory.**
2) **Figure to the right indicates full marks.**
3) **Use suitable data if necessary.**

SECTION - I

Q1) Answer any two. [16]

a) Explain Booth's algorithm with flowchart and example.

b) Draw and explain the flowchart for implementing twos compliment multiplier Control unit.

c) Explain OS services and components.

Q2) Attempt any Two. [16]

a) Explain the operating system services provided to user and to the system itself.

b) Design a complete Twos-complement 8 bit adder subtractor.

c) Explain register level design of a floating point adder pipeline

Q3) Attempt any three. [18]

a) Explain hard wired control with example.

b) Design 4 bit combinational Array Multiplier.

c) Explain the concept of multitasking.

d) Draw single precision and double precision micro instruction format.

P.T.O.

SECTION - II

Q4) Answer Any Two. **[18]**

a) What is process control block? Explain with suitable diagram.

b) Explain the various reasons for process termination.

c) Explain process state transition diagram with suspended state.

Q5) Answer Any Two. **[16]**

a) What is semaphore? Explain it's types.

b) Explain produces-consumer problem.

c) What is deadlock? Explain the conditions for deadlock.

Q6) Answer Any Two. **[16]**

a) What is memory partitioning? Explain dynamic Partitioning with the help of suitable diagram.

b) What is paging? Explain logical to physical address translation with the help of diagram.

c) What is segmentation? Explain segmentation with the help of suitable diagram.

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